

What is claimed:

1. A semiconductor package comprising:

a solder bumped semiconductor chip;

5 a surface metallized substrate, connected at said solder bumps to said solder bumped semiconductor chip; and,

a no-flow underfill surrounding connection points of said solder bumped semiconductor chip and said surface metallized substrate.

10 2. The solder bumped semiconductor chip of claim 1 wherein the solder bumps are composed of lead-tin Pb Sn alloy.

3. The solder bumped semiconductor chip of claim 1 wherein the solder bumps are composed of a single solder alloy.

15 4. The surface metallized substrate of claim 1 wherein the said substrate has a metallized patterned top surface.

5. The surface metallized substrate of claim 4 wherein the said substrate is ceramic.

20 6. The surface metallized substrate of claim 4 wherein the said substrate is epoxy.

7. The surface metallized substrate of claim 4 wherein the said substrate is any electrically insulating material that can be metallized.

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8. The surface metallized substrate of claim 4 wherein the patterned surface metallurgy is copper Cu.

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9. The surface metallized substrate of claim 4 wherein the patterned surface metallurgy is nickel Ni.

10. The surface metallized substrate of claim 4 wherein the patterned surface metallurgy has a gold Au flash on the top surface.

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11. The surface metallized substrate of claim 4 wherein the patterned surface is any electrically conductive metal.

12. The surface metallized substrate of claim 4 wherein the patterned surface metallurgy is formed by photolithographic processes.

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13. A method of fabricating a semiconductor package, the method comprising the steps of:
providing a semiconductor chip with a plurality of solder bumps on the surface;
providing a substrate with a metallized top surface;
disposing a no-flow underfill to the metallized surface of said surface metallized substrate;

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positioning said solder bumped semiconductor chip in contact with said surface metallized substrate to form an assembly;
curing the no-flow underfill; and

reflowing said assembly.

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14. The method of claim 13 wherein the curing process is in an inert environment.

15. The method in claim 13 wherein the reflow process is in an inert environment.

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